An Implementation of Quarter Pixel Block Motion Estimation Using SIMD*

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ABSTRACT

For improving video coding efficiency, sub-pixel motion estimation (ME) is used extensively in the existing video coding standards. The quarter pixel ME is one of the high complexity tools in H.264/AVC. In this paper, a parallel quarter block motion estimation algorithm that not only accelerates the process of sub-pixel motion estimation but also maintains accuracy as that of the original algorithm is proposed. In Intel P4 CPU, the SIMD (single instruction multiple data) technique is commonly used to provide an execution speedup. The implementation of this algorithm using parallel processing on P4 platform is discussed. The proposed algorithm satisfies in particular the requirements of low-rate real-timed video communication. Experimental results show that the optimized video encoder is more than 13.5 times faster than the original reference software while keeping the accuracy of the latter approximately.

Keywords: Sub-pixel Block Motion Estimation, Computation Complexity, Parallel Algorithm, SIMD, H.264/AVC

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