The Hardware Designing for Real Time FPGA Based Image Processing

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ABSTRACT

In this paper we present a high level software environment for FPGA-based image processing, which aims to hide hardware details as much as possible from the user. Our approach is to provide a very high level Image Processing Coprocessor with a core instruction set based on the operations of Image Algebra. The environment includes a generator which generates optimised architectures for specific user-defined operations.

Keywords: FPGA, Image, processing, DSP, Hardware.